Abstract of the Disclosure

A decoding system for multi-plane memories routes address information corresponding to distinct memory access operations to the designated planes. The system includes an array of functional registers dedicated to random access read, burst read, program, erase, and erase-suspend program operations. Plane selector blocks for each plane receive the address outputs from all of the registers and plane function select logic controls the routing in accord with memory access commands for specified planes. Simultaneous operations of different type in different planes and nested operations in the same plane are possible.